EM83040 LCD driver

1.General description

The EM83040 is a dot matrix LCD driver which is fabricated by low power CMOS technology. This chip includes 80- bits shift register , 80 bits data latch and 80 bits level driver. A LCD RAM inside can be mapping to LCD signal. It converts RAM data to parallel data and output lcd waveform to LCD.

2.Features

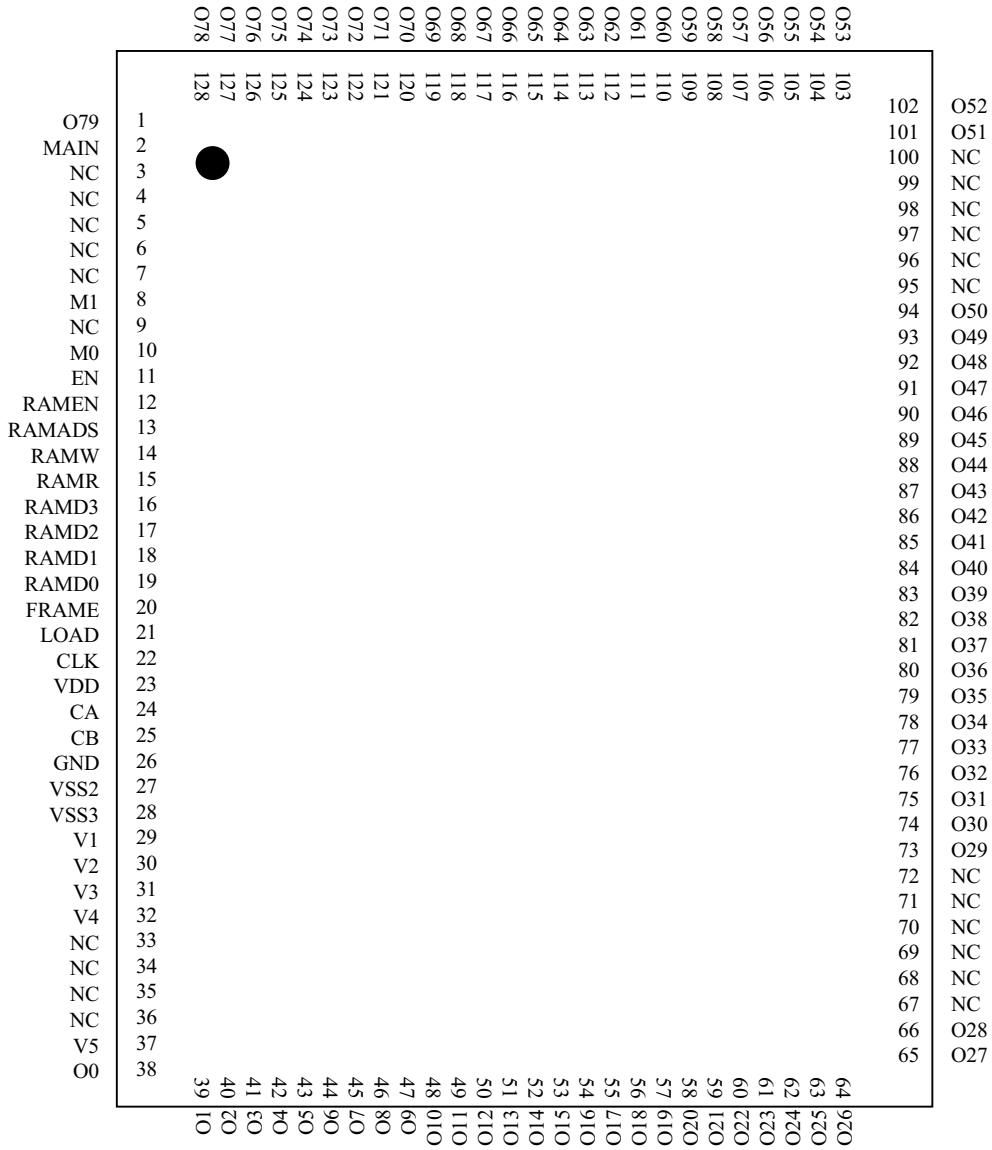
(1) Supply power 2.4~6V
(2) Internal RAM : 2.5k x 4 bits
(3) RAM can be controlled by eight signals including four bit data bus.
(4) LCD drive voltage :<18V
(5) Duty: 1/32, 1/48, 1/80
(6) Bias voltage can be supplied externally
(7) Build in DC converter double and triple
(8) Modularized function: connect to another 83040 to extent LCD matrix
(9) One DC converter enabled and other 83040 can shared with this.
(10) Chip form (EM83040H), 128 pin package (14mm x 20mm EM83040AQ), 160 pin package (EM83040BQ)

3.Application

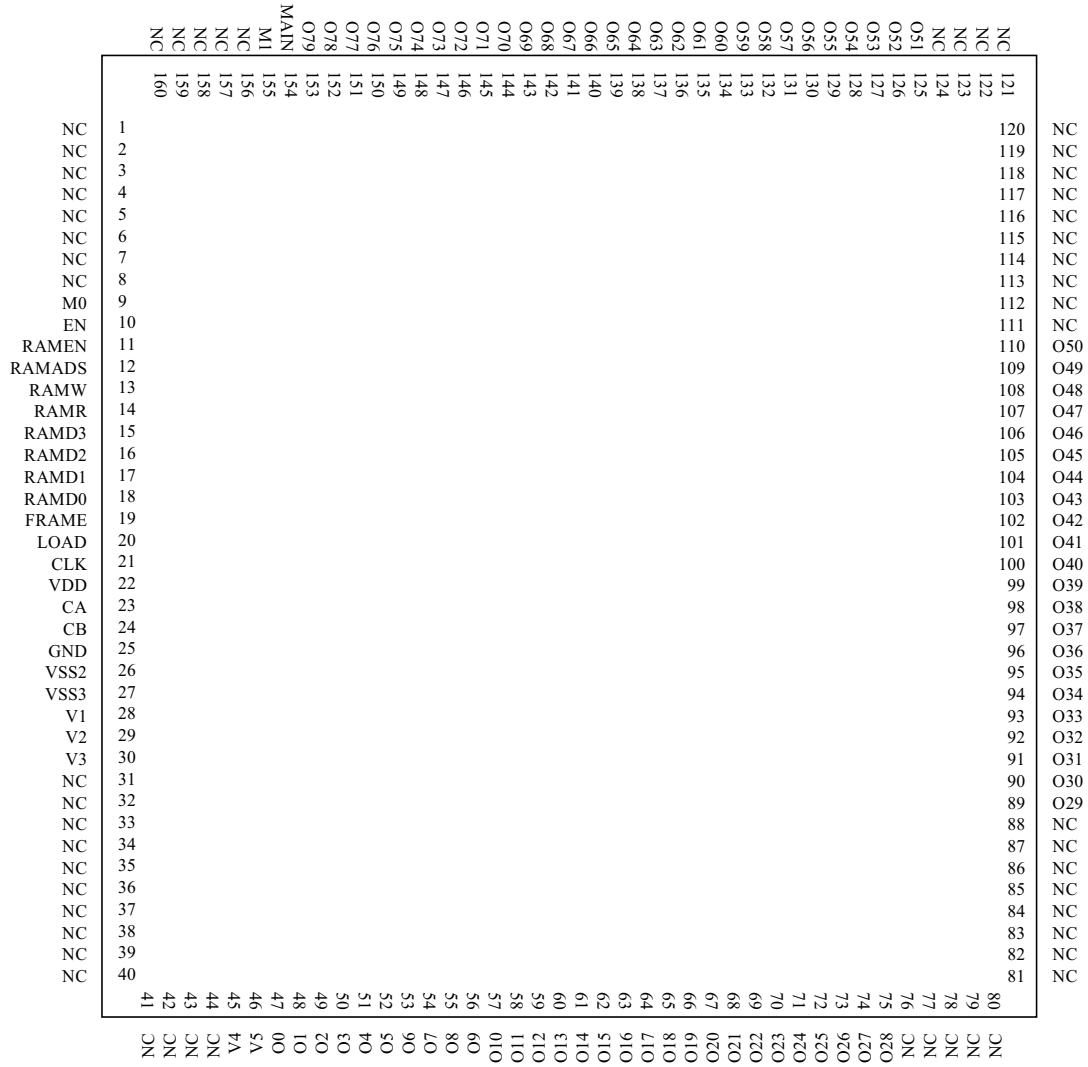
(1) Data Bank
(2) LCD toy
(3) Education computer

4.Pin assignment

EM83040AQ



EM83040BQ


NC 1
NC 2
NC 3
NC 4
NC 5
NC 6
NC 7
NC 8
M0 9
EN 10
RAMEN 11
RAMADS 12
RAMW 13
RAMR 14
RAMD3 15
RAMD2 16
RAMD1 17
RAMD0 18
FRAME 19
LOAD 20
CLK 21
VDD 22
CA 23
CB 24
GND 25
VSS2 26
VSS3 27
V1 28
V2 29
V3 30
NC 31
NC 32
NC 33
NC 34
NC 35
NC 36
NC 37
NC 38
NC 39
NC 40
41 NC
42 NC
43 NC
44 NC
45 V4
46 V5
47 O0
48 O1
49 O2
50 O3
51 O4
52 O5
53 O6
54 O7
55 O8
56 O9
57 O10
58 O11
59 O12
60 O13
61 O14
62 O15
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109 O49
110 O50
111 NC
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124 NC
125 O51
126 O52
127 O53
128 O54
129 O55
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131 O57
132 O58
133 O59
134 O60
135 O61
136 O62
137 O63
138 O64
139 O65
140 O66
141 O67
142 O68
143 O69
144 O70
145 O71
146 O72
147 O73
148 O74
149 O75
150 O76
151 O77
152 O78
153 O79
154 MAIN
155 M1
156 NC
157 NC
158 NC
159 NC
160 NC

5.Block diagram

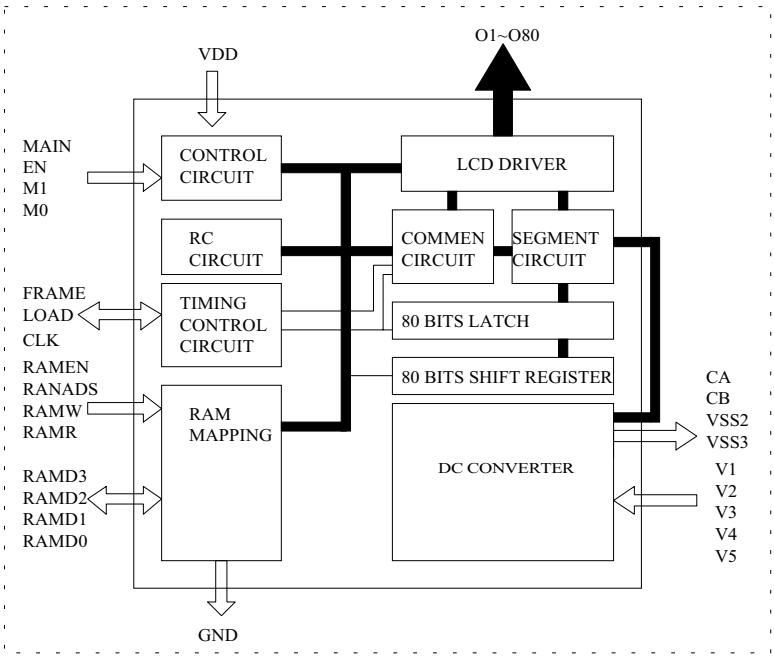


Fig2

6.Pin description

VDD	Power	
GND	power	Ground
VSS3	Power	EN=0 and MAIN=1, 2*VDD output, EN=1 ,VSS3=VDD
VSS2	Power	EN=0 and MAIN=1, 3*VDD output, EN=1, VSS2=VDD
MAIN	I	Master or slave control signal. MAIN=1 ,master unit MAIN=0 , slave unit
EN	I	This pin control whole chip power. This chip will work when this pin is connectted to ground. And whole chip will disable when connect to VDD voltage. EN=0 and MAIN=1 the chip will generate VSS2, VSS3, FRAME, LOAD, CLK signal and internal RC clock. EN=1, standby mode
M1	I	Mode select
M0	I	Mode select
RAMEN		RAM read and write control signal. 1 => can not read and write. 0=> can read and write.
RAMADS		RAM data select signal 1=> RAM Data , 0=>Address
RAMW		RAM write signal, low write
RAMR		RAM read signal, low read
RAMD3~RAMD0		RAM data or address bus
CLK	I/O	System clock. MAIN=1 , the master unit will output system clock. MAIN=0 , the slave will accept the clock from master unit.
LOAD	I/O	LCD load signal between one COMMON signal to another . MAIN=1 , the master unit will output LOAD signal. MAIN=0 , the slave will accept the signal from master unit.
FRAME	I/O	LCD frame control . MAIN=1 , the master unit will output FRAME signal. MAIN=0 , the slave will accept the signal from master unit.
CA	I	Coupling capacitor
CB	I	Coupling capacitor
V1~V5	I	Reference voltage input ,highest V1..lowest V5
O1~O80	O	LCD waveform output

7.Function description

(1)User can use MAIN pin to chose master unit or slave unit.

MAIN	Unit	Function
1	MASTER	Generate these signals Clk, Frame, Load, VSS2, VSS3, Internal RC clock
0	SLAVE	Accept these signals Clk, Frame, Load, V1, V2, V3, V4, V5

(2)User can use M1,M2 to chose four modes. As followed

MASTER	MAIN	M1	M0	Segment	Common	Ps.
Mode1	1	0	0	Reserved for test		
Mode2	1	0	1		O(80:1)=C(80:1)	
Mode3	1	1	0	O(32:1)=S(32:1)	O(80:33)=C(48:1)	
Mode4	1	1	1	O(48;1)=S(48:1)	O(80:49)=C(32:1)	
SLAVE	MAIN	M1	M0	Segment	Common	Ps.
Mode1	0	0	0	Reserved for test		**M1, M0 should as same as master unit**
Mode2	0	0	1	O(80:1)=S(80:1)		
Mode3	0	1	0	O(80:1)=S(80:1)		
Mode4	0	1	1	O(80:1)=S(80:1)		
				Ps: S=segment	C=common	

(3)RAM control

Write mode

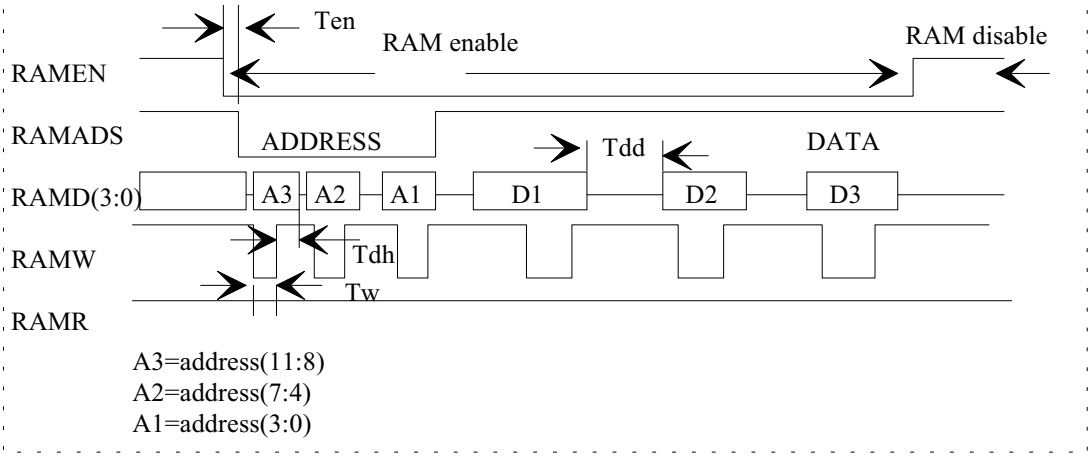


Fig3

LCD RAM can be written or read with control signal. The RAMEN pin can select a RAM which can be read or write . The RAMADS pin can select whether RAMD(3:0) are data or address of RAM. At the address mode ,RAMADS is low and user should sent address three times. From address (11:8) to address (3:0). Then it will go into data mode when RAMADS is high. In data mode , user can sent one or more nibble data which address can be increased by internal counter.

Once the RAMEN pin is high, the RAM can not read and write.

(4)read mode

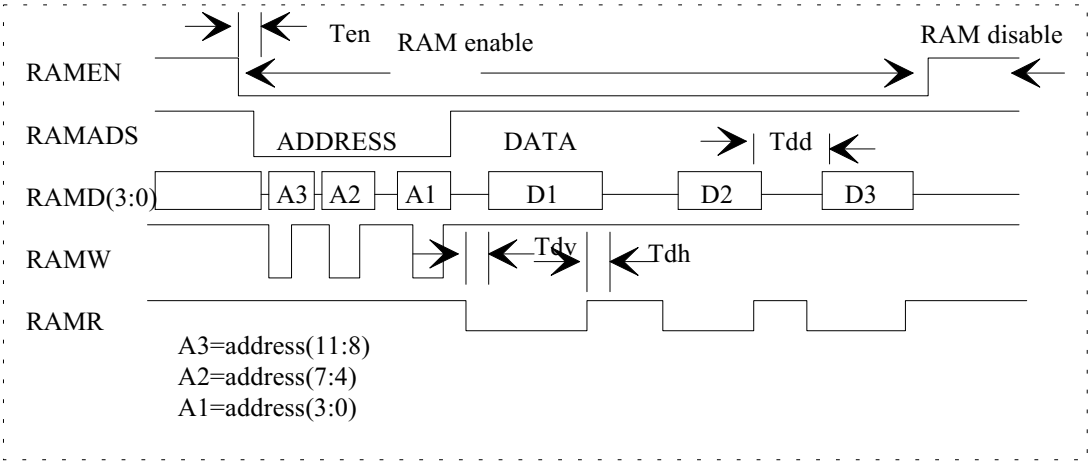


fig4

As same as write mode , user has to sent address three times. And read data from RAM one by one which address can be increased by internal counter. Note!! Be sure to make RAMR low pulse 2 u S (Tdv +data) width and 2 u S (Tdd) high width at least.

(5)RAM mapping

RAM address is from 0 to address 2559

User fill “1” to LCD RAM , LCD driver will generate “light” waveform. Otherwise , it will generate a “dark” waveform. The LCD RAM area is mapped to segment 1 to segment 80 from address 0 to address 19. And user can refer to fig.5 to get the idea of

address2559 ……	address2547…… address2528	COM80
GENERAL RAM	LCD RAM	
address0063 ……	address0039 …… address0032	COM2
address0031 ……	address0019 …… address0000	COM1
	b3 b2 b1 b0 b3 b2 b1 b0	
	s80s79s78s77 s4 s3 s2 s1	

LCD ram mapping. The other RAM can use as general RAM for data storage.

Fig5

(6)LCD waveform

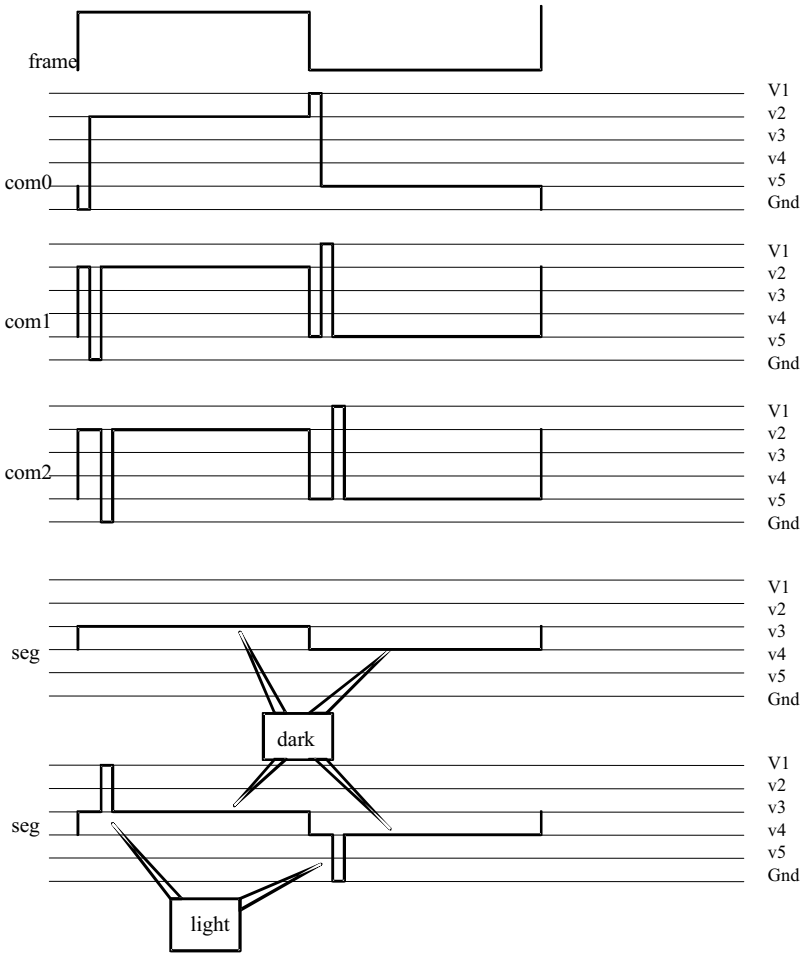


Fig6

8.Absolute rating

RATING	SYMBOL	VALUE	UNIT
DC SUPPLY VOLTAGE	V+	<6	V
INPUT VOLTAGE	Vin	-0.5 TO Vdd +0.5	V
OPERATING TEMPERATURE RANGE	Ta	0 TO 70	℃

9.DC characteristic

(Ta=0°C ~ 70°C, VDD=3V±5%, VSS=0V)

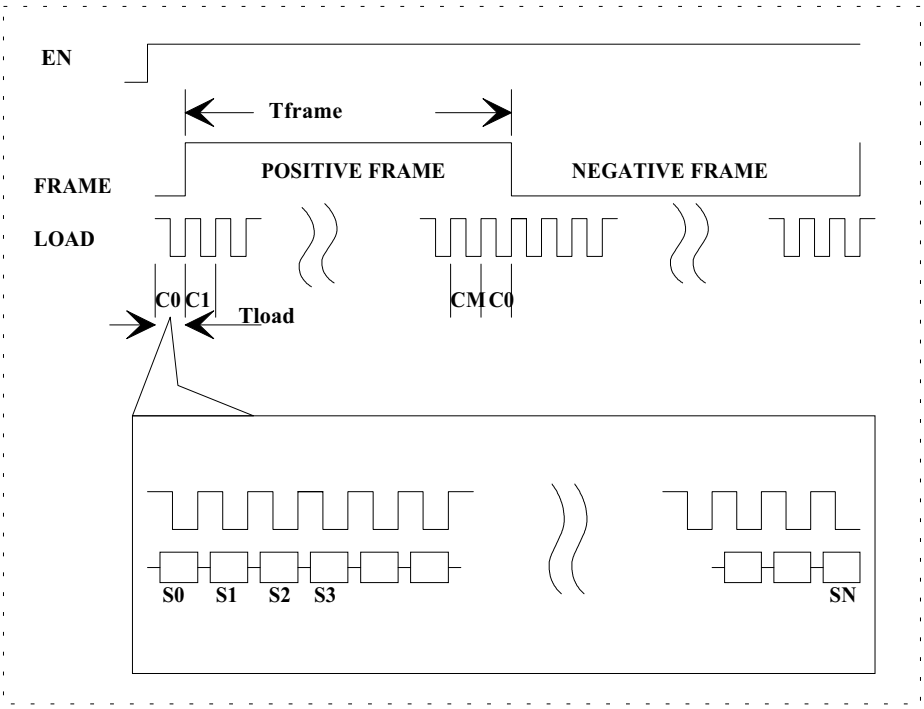
Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH	Input High Voltage		2.0			V
VIL	Input Low Voltage				0.8	V
Ioh	Output High current	VDD=3V	100			μA
Iol	Output low current	VDD=3V	-100			μA
Isd	Standby current	EN=1		1	4	μA
Iop	Operating current	EN=0 . MAIN =1 (MASTER) , DC converter enable, 1MHz clock INPUT=VDD		400	600	μA
		EN=0 . MAIN =0 (SLAVE) , DC converter disable, 1MHz clock INPUT = VDD		100	150	μA

10. AC Characteristic

(Ta=0°C ~ 70°C, VDD=3V, VSS=0V)

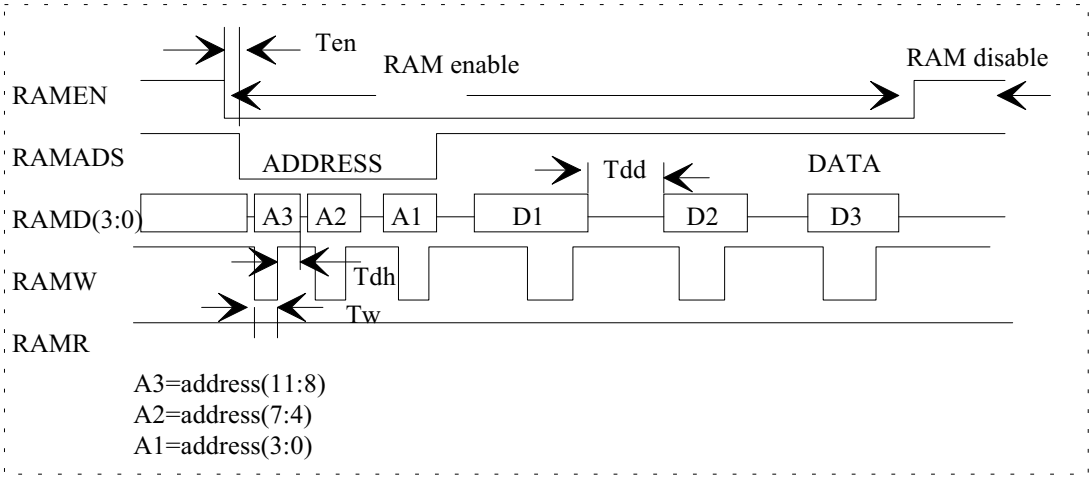
Symbol	Parameter	Min	Typ	Max	Unit
Tframe	Frame period		1/64		S
Tload	Load period		31		uS
Ten	Enable time	30			uS
Tw	Write low pulse	2			uS
Tdh	Data hold time	500			nS
Tdd	Data to data time	2			uS
Tdv	Data valid time	1500			nS

11. AC timing



LCD contrl timing

Fig7



LCD RAM write mode

Fig8

LCD RAM read mode

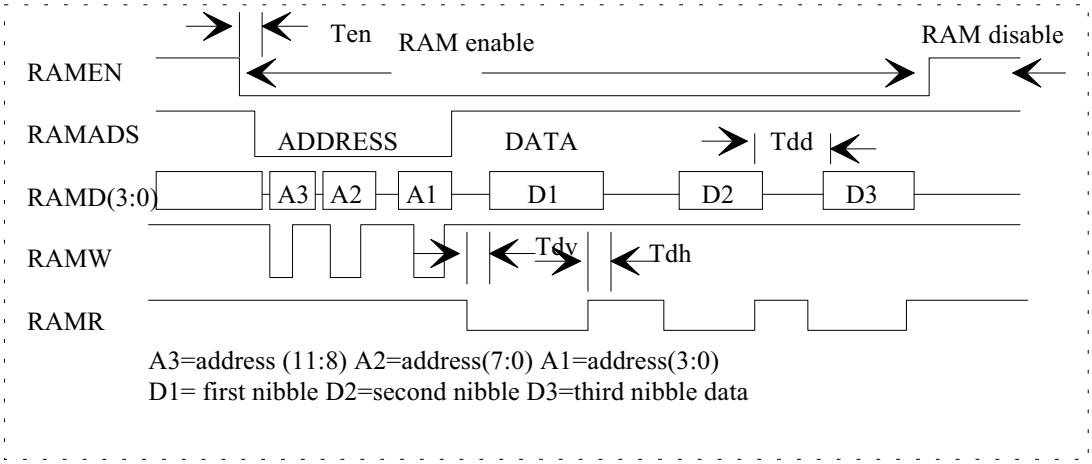


Fig9

12. Application circuit

(1),C32 x S48, 78861+83040

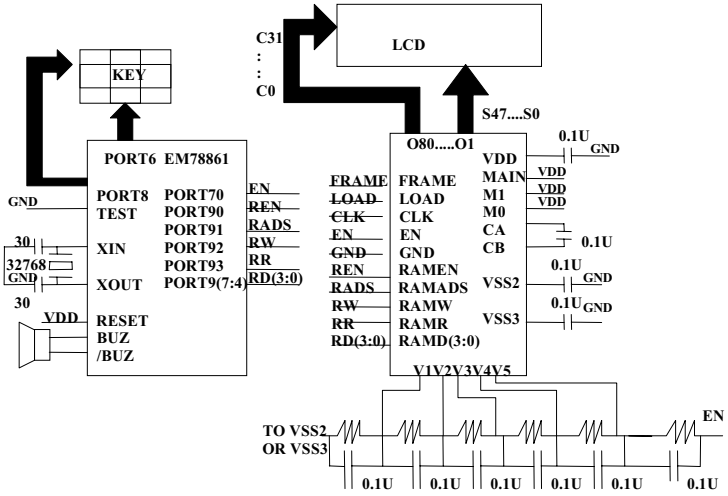


fig10

(2),C32 x S128, 78861 +83040+83040

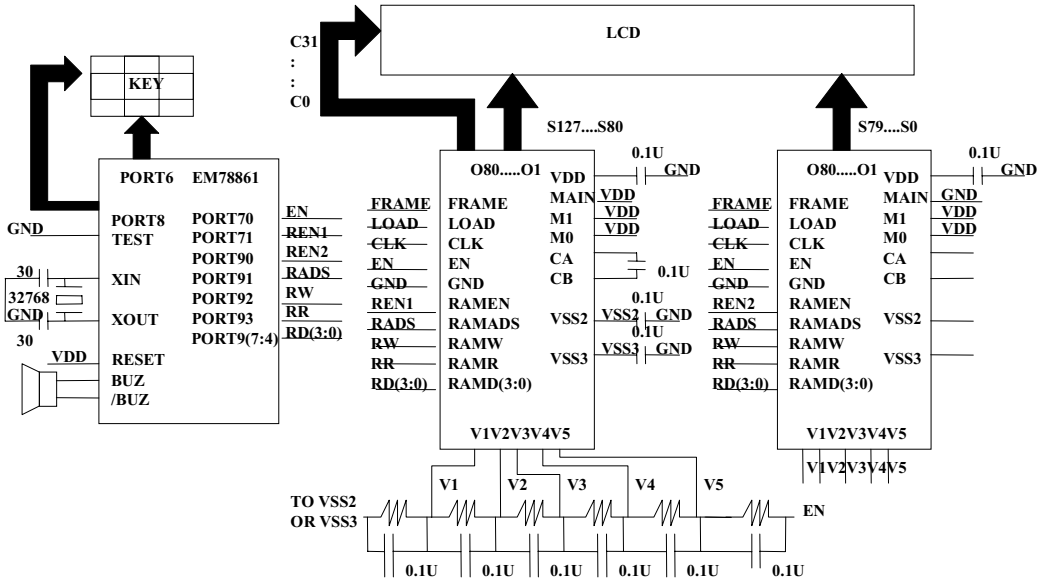


fig11

(3), C48 x S112, 78861 +83040 +83040

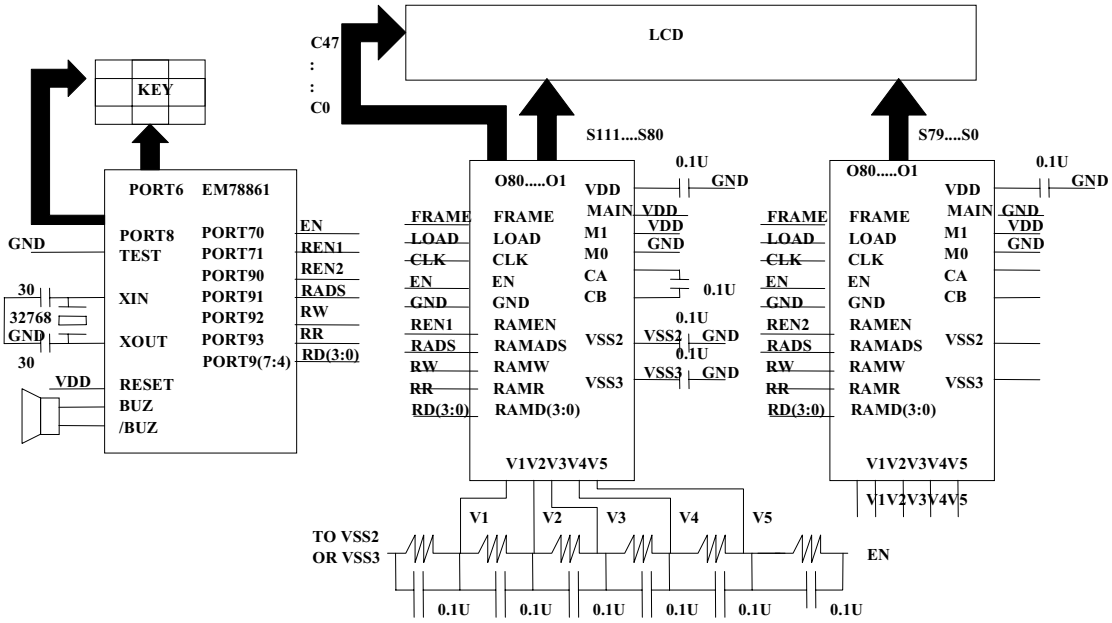


fig12

(4) C80 x S160, 78861 + 83040 +83040 +83040

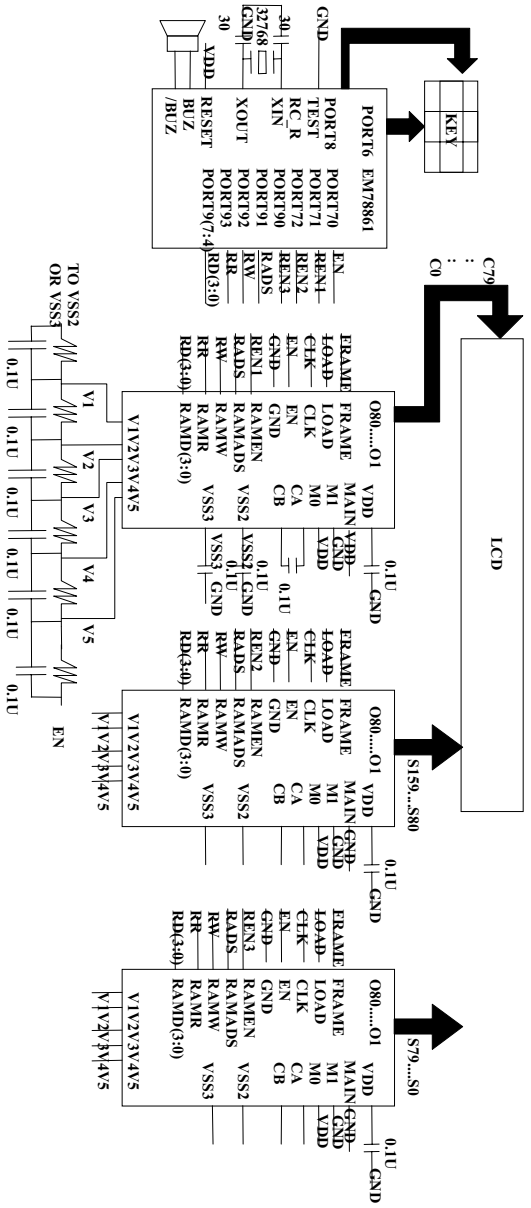
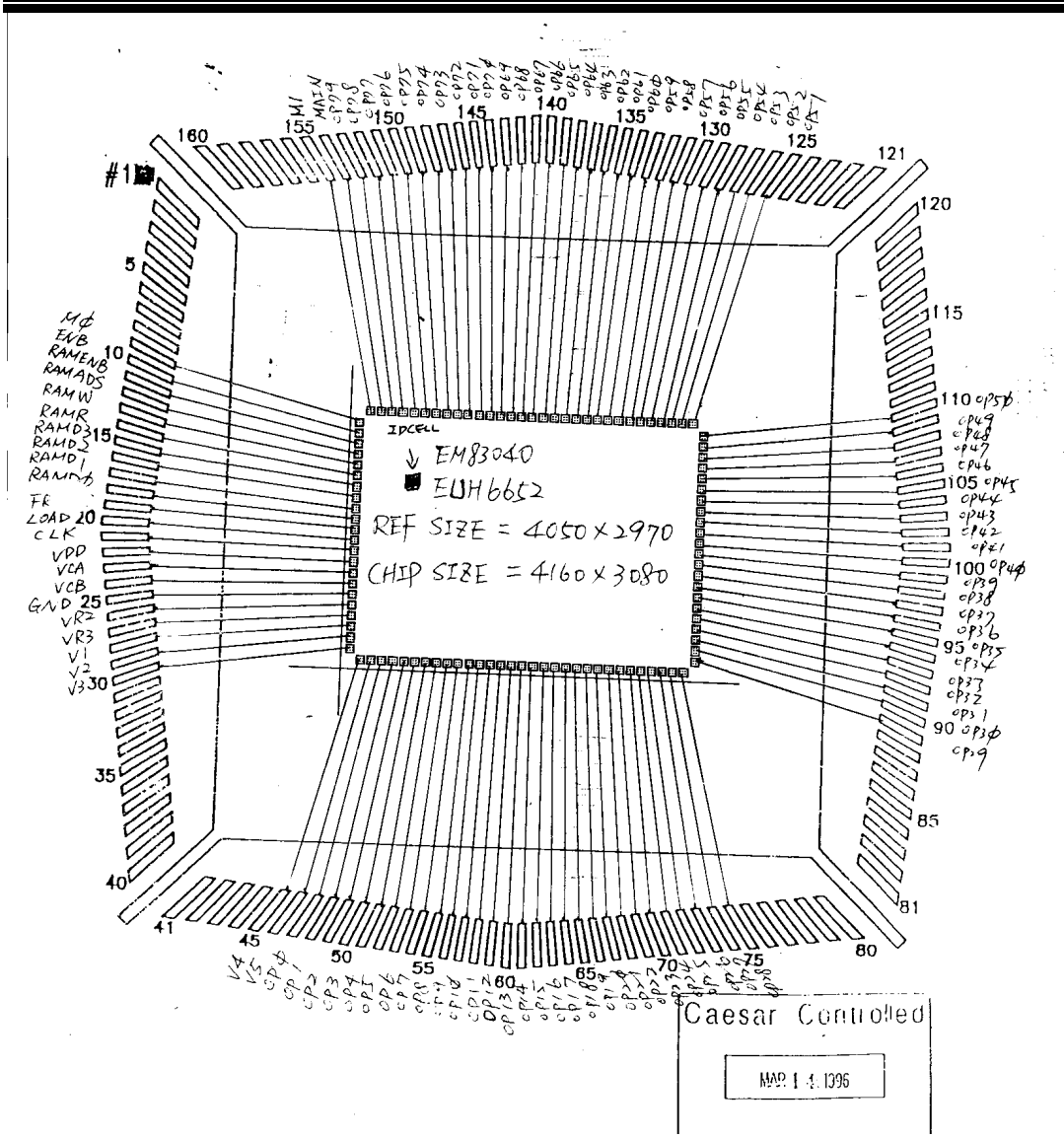


Fig13


IDCELL
EM83040
EUH6652
REF SIZE = 4050 × 2970
CHIP SIZE = 4160 × 3080
Caesar Controlled
MAR 1 4 1996

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
1		
2		
3		
4		
5		
6		
7		
8		
9	M0	-1920.0 ,1260.0
10	ENB	-1920.0 ,1140.0
11	RAMENB	-1920.0 ,1020.0
12	RAMADS	-1920.0 ,900.0
13	RAMW	-1920.0 ,780.0
14	RAMR	-1920.0 ,660.0
15	RAMD_3_	-1920.0 ,540.0
16	RAMD_2_	-1920.0 ,420.0
17	RAMD_1_	-1920.0 ,300.0
18	RAMD_0_	-1920.0 ,180.0
19	FRAME	-1920.0 ,60.0
20	LOAD	-1920.0 ,-60.0
21	CLK	-1920.0 ,-180.0
22	VDD	-1920.0 ,-300.0
23	VCA	-1920.0 ,-420.0
24	VCB	-1920.0 ,-540.0
25	GND	-1920.0 ,-660.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
26	VR2	-1920.0 ,-780.0
27	VR3	-1920.0 ,-900.0
28	V1	-1920.0 ,-1020.0
29	V2	-1920.0 ,-1140.0
30	V3	-1920.0 ,-1260.0
31		
32		
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38		
39		
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43		
44		
45	V4	-1800.0 ,-1380.0
46	V5	-1680.0 ,-1380.0
47	OP_0_	-1560.0 ,-1380.0
48	OP_1_	-1440.0 ,-1380.0
49	OP_2_	-1320.0 ,-1380.0
50	OP_3_	-1200.0 ,-1380.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
51	OP_4_	-1080.0 ,-1380.0
52	OP_5_	-960.0 ,-1380.0
53	OP_6_	-840.0 ,-1380.0
54	OP_7_	-720.0 ,-1380.0
55	OP_8_	-600.0 ,-1380.0
56	OP_9_	-480.0 ,-1380.0
57	OP_10_	-360.0 ,-1380.0
58	OP_11_	-240.0 ,-1380.0
59	OP_12_	-120.0 ,-1380.0
60	OP_13_	0.0 ,-1380.0
61	OP_14_	120.0 ,-1380.0
62	OP_15_	240.0 ,-1380.0
63	OP_16_	360.0 ,-1380.0
64	OP_17_	480.0 ,-1380.0
65	OP_18_	600.0 ,-1380.0
66	OP_19_	720.0 ,-1380.0
67	OP_20_	840.0 ,-1380.0
68	OP_21_	960.0 ,-1380.0
69	OP_22_	1080.0 ,-1380.0
70	OP_23_	1200.0 ,-1380.0
71	OP_24_	1320.0 ,-1380.0
72	OP_25_	1440.0 ,-1380.0
73	OP_26_	1560.0 ,-1380.0
74	OP_27_	1680.0 ,-1380.0
75	OP_28_	1800.0 ,-1380.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
76		
77		
78		
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81		
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84		
85		
86		
87		
88		
89	OP_29_	1920.0 ,-1260.0
90	OP_30_	1920.0 ,-1140.0
91	OP_31_	1920.0 ,-1020.0
92	OP_32_	1920.0 ,-900.0
93	OP_33_	1920.0 ,-780.0
94	OP_34_	1920.0 ,-660.0
95	OP_35_	1920.0 ,-540.0
96	OP_36_	1920.0 ,-420.0
97	OP_37_	1920.0 ,-300.0
98	OP_38_	1920.0 ,-180.0
99	OP_39_	1920.0 ,-60.0
100	OP_40_	1920.0 ,60.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
101	OP_41_	1920.0 ,180.0
102	OP_42_	1920.0 ,300.0
103	OP_43_	1920.0 ,420.0
104	OP_44_	1920.0 ,540.0
105	OP_45_	1920.0 ,660.0
106	OP_46_	1920.0 ,780.0
107	OP_47_	1920.0 ,900.0
108	OP_48_	1920.0 ,1020.0
109	OP_49_	1920.0 ,1140.0
110	OP_50_	1920.0 ,1260.0
111		
112		
113		
114		
115		
116		
117		
118		
119		
120		
121		
122		
123		
124		
125	OP_51_	1800.0 ,1380.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
126	OP_52_	1680.0 ,1380.0
127	OP_53_	1560.0 ,1380.0
128	OP_54_	1440.0 ,1380.0
129	OP_55_	1320.0 ,1380.0
130	OP_56_	1200.0 ,1380.0
131	OP_57_	1080.0 ,1380.0
132	OP_58_	960.0 ,1380.0
133	OP_59_	840.0 ,1380.0
134	OP_60_	720.0 ,1380.0
135	OP_61_	600.0 ,1380.0
136	OP_62_	480.0 ,1380.0
137	OP_63_	360.0 ,1380.0
138	OP_64_	240.0 ,1380.0
139	OP_65_	120.0 ,1380.0
140	OP_66_	0.0 ,1380.0
141	OP_67_	-120.0 ,1380.0
142	OP_68_	-240.0 ,1380.0
143	OP_69_	-360.0 ,1380.0
144	OP_70_	-480.0 ,1380.0
145	OP_71_	-600.0 ,1380.0
146	OP_72_	-720.0 ,1380.0
147	OP_73_	-840.0 ,1380.0
148	OP_74_	-960.0 ,1380.0
149	OP_75_	-1080.0 ,1380.0
150	OP_76_	-1200.0 ,1380.0

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)
151	OP_77_	-1320.0 ,1380.0
152	OP_78_	-1440.0 ,1380.0
153	OP_79_	-1560.0 ,1380.0
154	MAIN	-1680.0 ,1380.0
155	M1	-1800.0 ,1380.0
156		
157		
158		
159		
160		

euh6652 Pad Name & Cordinates Table		
Structure Name: EUH6652 Chip Size: 4160 * 3080 UM		
Pin No	Pad Name	Coordinate (X , Y)